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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. MIO 012 V2 Total Pages

First Named Inventor or Application Identifier

Howard E. Rhodes

Express Mail Label No.

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1.  Fee Transmittal Form  
(Submit an original, and a duplicate for fee processing)

2.  Specification [Total Pages 22]  
(preferred arrangement set forth below)

- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3.  Drawing(s) (35 USC 113) [Total Sheets 9]

4. Oath or Declaration [Total Pages 2]
 

- a.  Newly executed (original or copy)
- b.  Copy from a prior application (37 CFR 1.63(d))  
(for continuation/divisional with Box 17 completed)  
(Note Box 5 below)
  - i.  DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5.  Incorporation By Reference (useable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO: Assistant Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

6.  Microfiche Computer Program (Appendix)

7. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
 

- a.  Computer Readable Copy
- b.  Paper Copy (identical to computer copy)
- c.  Statement verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

8.  Assignment Papers (cover sheet & document(s))

9.  37 CFR 3.73(b) Statement  Power of Attorney  
(when there is an assignee)

10.  English Translation Document (if applicable)

11.  Information Disclosure Statement (IDS)/PTO-1449  Copies of IDS Citations

12.  Preliminary Amendment

13.  Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)

14.  Small Entity  Statement filed in prior application, Statement(s)  Status still proper and desired

15.  Certified Copy of Priority Document(s)  
(if foreign priority is claimed)

16.  Other: Check \$790.00(filing fee)  
.....  
.....

## 17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

 Continuation     Divisional     Continuation-in-part (CIP)    of prior application No: 08 / 789,072
**18. CORRESPONDENCE ADDRESS**
 Customer Number or Bar Code Label XXXXXXXXXX or  Correspondence address below

(Insert Customer No. or Attach bar code label here)

NAME	Timothy W. Hagan			
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**FEE TRANSMITTAL**

*Note: Effective October 1, 1997.  
Patent fees are subject to annual revision.*

TOTAL AMOUNT OF PAYMENT (\$ 790.00)

*Complete if Known*

Application Number	
Filing Date	
First Named Inventor	Howard E. Rhodes
Group Art Unit	
Examiner Name	
Attorney Docket Number	MTO 012 V2

**METHOD OF PAYMENT** (check one)

1.  The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number   
Deposit Account Name

Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17       Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2.  Payment Enclosed:  
 Check     Money Order     Other

**FEE CALCULATION****1. FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 790	201 395	Utility filing fee	790
106 330	206 165	Design filing fee	
107 540	207 270	Plant filing fee	
108 790	208 395	Reissue filing fee	
114 150	214 75	Provisional filing fee	
SUBTOTAL (1) (\$ 790)			

**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 400	216 200	Extension for reply within second month	
117 950	217 475	Extension for reply within third month	
118 1,510	218 755	Extension for reply within fourth month	
128 2,060	228 1,030	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,320	241 660	Petition to revive - unintentional	
142 1,320	242 660	Utility issue fee (or reissue)	
143 450	243 225	Design issue fee	
144 670	244 335	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
149 790	249 395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify) _____			
Other fee (specify) _____			
* Reduced by Basic Filing Fee Paid			SUBTOTAL (3) (\$ 0)

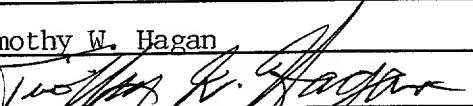
**2. CLAIMS**

Total Claims	10	-20	= 0	X 22	= -0-
Independent Claims	2	- 3	= 0	X 82	= -0-
Multiple Dependent Claims	0		X 270	= -0-	

**Large Entity Small Entity**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 22	203 11	Claims in excess of 20
102 82	202 41	Independent claims in excess of 3
104 270	204 135	Multiple dependent claim
109 82	209 41	Reissue independent claims over original patent
110 22	210 11	Reissue claims in excess of 20 and over original patent
SUBTOTAL (2) (\$ 0)		

Complete (if applicable)

Typed or Printed Name	Timothy W. Hagan	Reg. Number	29,001
Signature		Date	1-13-98
		Deposit Account User ID	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants : Howard Rhodes, Luan Tran  
Serial No. :  
Filed :  
Title : METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING  
        IMPROVED CONTACTS TO A THIN CONDUCTIVE LAYER  
Examiner : T. Thomas  
Art Unit : 1104  
Docket : MIO 012 V2 (94-0112.04)

Assistant Commissioner for  
Patents  
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

This preliminary amendment is being filed to present claims which were the subject of a restriction requirement made in the grandparent of this application. Examination and favorable consideration are respectfully requested.

IN THE SPECIFICATION

At pages 1 and 2, please change the Title to read:

-- METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING IMPROVED  
CONTACTS TO A THIN CONDUCTIVE LAYER --.

At page 2, after the Title, please insert the following:

-- CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. Patent Application Serial No. 08/789,072, filed February 3, 1997, which application was a file-wrapper-continuing application of U.S. Patent Application Serial No. 08/399,844, filed March 7, 1995, now abandoned. This application is also related to U.S. Patent Application Serial No. 08/733,340, filed October 17, 1996. --

IN THE CLAIMS

Please cancel claims 1 - 20 in the application and replace them with new claims 21 - 30 below prior to calculating the filing fee.

21. A process for making a semiconductor device comprising the steps of:  
    forming a layer of conductive material having a topography that includes a substantially vertical component; and  
    forming a contact disposed adjacent to and contacting said vertical component.
22. A process as claimed in claim 21 wherein said vertical component defines a localized thick region in the layer of conductive material.
23. A process as claimed in claim 21 wherein said vertical component is a spacer.
24. A process as claimed in claim 21 further comprising the step of forming a structure having an opening therein under said conductive layer and filling said opening with said conductive material to form said vertical component.
25. A process as claimed in claim 21 wherein said conductive layer is a capacitor electrode.
26. A process for making a semiconductor device having an improved contact to a conductive layer comprising the steps of:  
    providing a first layer of material and forming an opening therein, said opening including sidewalls;  
    5     forming a layer of a first conductive material on said first layer of material and along the surfaces of said sidewalls of said opening to form a localized thick region;  
    forming an overlayer of material on said layer of said first conductive material;  
    forming a contact hole in said overlayer which communicates with said layer of said first conductive material; and

substantially filling said contact hole in said overlayer with a second conductive material which differs in composition from said first conductive layer and which contacts said first conductive material.

27. A process as claimed in claim 26 in which said first conductive material forms spacers on said sidewalls of said opening.

28. A process as claimed in claim 27 in which said second conductive material contacts at least said spacers.

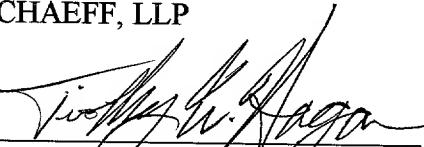
29. A process as claimed in claim 26 in which said first conductive material comprises polysilicon and said second conductive material comprises a metal.

30. A process as claimed in claim 26 in which said first layer and said overlayer comprise insulating materials.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN  
& SCHAEFF, LLP

By



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ATTORNEY  
DOCKET NO. 94-112

SEMICONDUCTOR DEVICE HAVING IMPROVED  
CONTACTS TO A THIN CONDUCTIVE LAYER  
AND PROCESS FOR MAKING SAID DEVICE

INVENTOR:

HOWARD E. RHODES

Inventor(s): H. Rhodes

**SEMICONDUCTOR DEVICE HAVING IMPROVED  
CONTACTS TO A THIN CONDUCTIVE LAYER  
AND PROCESS FOR MAKING SAID DEVICE**

Field of the Invention

The invention relates generally to the formation of a semiconductor device and process for making the device and, more particularly, to a semiconductor device having a localized thick region in a thin conductive layer for making electrical contact to a conductor.

Background of the Invention

Generally, semiconductor devices are formed by alternately stacking layers of conducting and insulating materials over a semiconductor substrate. Contact holes are etched through some or all of these layers at specific locations and, thereafter, metal conductors are deposited into the holes to provide for electrical contact to external circuits. Contact holes are typically etched down to active areas on the surface of the substrate or to an intervening conductive layer. Variations in the thickness of the layers of material, non-uniformity of the film deposition and planarizing processes and limitations inherent in the etching process make it difficult to ensure the contact hole will stop precisely on the conductive layer to which contact will be made. This is particularly true as the conductive layers are made thinner for the increasingly small memory cell components currently being incorporated into random access semiconductor memory devices. Where contact must be made to a conductive layer that is thin in comparison to the overlaying materials through which the contact hole is etched, the contact hole etch must be precisely controlled to maximize the chances the hole stops on the thin conductive layer.

The problems associated with forming reliable contacts to a thin conductive layer are illustrated below where I have

Inventor(s): H. Rhodes

described part of a process for manufacturing a conventional stacked capacitor DRAM. Fig. 1 shows the structure of a conventional stacked capacitor DRAM after formation of the capacitor top electrode, also commonly referred to as the "cell poly." Cell poly 2 is a layer of doped polysilicon formed over dielectric layer 4, capacitor bottom electrode 6, field effect transistor gate electrode 8, and substrate 10.

Referring to Fig. 2, upper insulating layer 12 is stacked over substrate 10. Upper insulating layer 12 is etched to form a contact hole 14 which, ideally, extends just down to cell poly 2. In order to minimize the number of manufacturing process steps, this contact hole etch is typically performed as part of the same etch that forms bit line contact 15. Contact hole 14 is then filled with a metal conductor 16 for electrically connecting the cell poly to an external voltage source.

Upper insulating layer 12 and cell poly 2 are typically about 20,000 Angstroms and 1,000 Angstroms thick, respectively. The thickness of upper insulating layer 12 may vary from place to place due to the stepped substrate materials over which it is formed and non-uniformity of the film deposition and planarizing processes. Also, the contact hole etch must continue long enough to expose the deepest contact, bit line contact 15 in this example, at the thickest part of upper insulating layer 12. Hence, the contact hole will be over etched into and sometimes through the thin cell poly as illustrated in Fig. 3A. Etching through cell poly 2 diminishes the effectiveness of the cell poly/metal contact by forming a sidewall contact causing undesirable high contact resistance between conductor 16 and cell poly 2. Where the cell poly is formed in close proximity to the substrate, as shown in Fig. 3B, etching through cell poly 2 causes electrical shorting of cell poly 2 to substrate 10 through conductor 16.

Inventor(s) : H. Rhodes

Current methods to reduce the risk of over etching the cell poly contact hole include precisely controlled etch times and the development and use of highly selectively etch processes. Adequate selectivity is difficult to achieve, however, as device geometries shrink, bit line contacts become deeper and the cell poly becomes thinner.

One solution to the problem of shorting a thin conductive layer (described above for the cell poly) is disclosed in U.S. Patent No. 5,243,219, issued to Katayama on September 7, 1993. Katayama discloses an impurity diffused region in the substrate directly below the contact hole. The resulting pn junction between the impurity diffused region and the substrate isolates the conductive layer from the substrate in the event the contact hole is etched through the thin conductive layer. Although the device of Katayama minimizes some of the undesirable effects of etching through the thin conductive layer, it does not eliminate this fundamental problem which is inherent in the formation of reliable contacts to a thin conductive layer.

There remains a need for a structure and manufacturing process that lessens or eliminates the risk of etching the contact hole through a thin conductive layer. It is desirable that such structure and process be of practical use in a variety of semiconductor device applications, including those in which the conductive layer is remote from the substrate.

#### Summary of the Invention

One object of the invention is to provide an improved contact to a relatively thin conductive layer.

Another object of the invention is to lessen the risk of etching the contact hole through the conductive layer to which contact will be made.

Another object is to prevent a shorting path or current leakage between the metal contact and underlying conductive or semiconductive materials.

Inventor(s): H. Rhodes

According to the present invention, these and other objects are achieved by a semiconductor device having a conductive layer with a localized thick region positioned below the contact hole. In one embodiment of the invention, the thick region to which contact is made is formed by means of an opening in an underlayer of material. In this embodiment, the device includes an underlayer of material having an opening therein; a layer of thin conductive material formed on the underlayer and in the opening; an overlayer of material having a contact hole therethrough formed on the layer of thin conductive material; a conductor contacting the layer of thin conductive material through the contact hole; and wherein the opening in the underlayer is positioned below the contact hole and sized and shaped to form a localized thick region in the layer of thin conductive material within the opening.

In another embodiment, the invention is incorporated into a stacked capacitor DRAM. In this embodiment, the semiconductor device includes a field effect transistor formed in a memory cell array region of a semiconductor substrate, the field effect transistor having a gate electrode formed over the substrate, and first and second source/drain regions formed in the surface of the substrate on opposite sides of the gate electrode; a capacitor formed in the memory cell array region, the capacitor comprising a bottom electrode formed over the substrate in electrical contact with the first source/drain region, a dielectric layer formed on the bottom electrode, and a first region of a polysilicon top electrode formed on the dielectric over the bottom electrode; a second region of the polysilicon top electrode formed in a peripheral region of the substrate adjacent to the memory cell array region; an underlayer of material interposed between the substrate and the second region of the polysilicon top electrode in the peripheral region; an opening in the underlayer; an insulating layer formed on the second region of

Inventor(s): H. Rhodes

the polysilicon top electrode; a contact hole through the insulating layer; a conductor contacting the second region of the polysilicon top electrode through the contact hole; and wherein the opening in the underlayer is positioned below the contact hole.

A process for making a semiconductor device according to the invention includes the steps of: forming a first layer of thin conductive material; forming a second layer of material having a contact hole therethrough on the first layer; forming a localized thick region in the first layer and positioning the thick region below the contact hole; and forming a conductor contacting the thick region through the contact hole.

The semiconductor device of the invention, wherein the conductive layer has a localized thick region formed and positioned directly below the contact hole, eliminates the risk of etching the contact hole through the conductive layer, improves the conductive layer/conductor contact and prevents current leakage between the conductor and the substrate or other structure underlying the conductive layer.

Additional objects, advantages and novel features of the invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figs. 1 and 2 are cross sectional views of a portion of a conventional stacked capacitor DRAM at various stages of formation.

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Fig. 3A is a cross sectional view of a portion of a conventional stacked capacitor DRAM showing the contact hole etched through the cell poly.

Fig. 3B is a cross sectional view of a portion of a conventional stacked capacitor DRAM showing the contact hole etched through the cell poly with the cell poly in close proximity to the substrate.

Figs. 4-7 are cross sectional views illustrating the general structure of one of the preferred embodiments of the invention at various stages of formation.

Figs. 8-9 are cross sectional views illustrating another embodiment of the invention wherein the conductive layer/conductor contact is formed along a sidewall of the opening in the underlayer. The cross sectional view of Fig. 9 is taken along the line 1-1 in Fig. 10.

Fig. 10 is a top down plan view of the structure of Fig. 9, except that overlayer 28 in Fig. 9 is omitted, wherein the conductive layer/conductor contact is formed along a sidewall of the opening in the underlayer.

Figs. 11-16 illustrate another preferred embodiment wherein the invention is incorporated into a stacked capacitor DRAM.

The figures are not meant to be actual views of the various embodiments, but merely idealized representations used to depict the structure and process of the invention.

#### Detailed Description of the Preferred Embodiments —

The fabrication of semiconductor devices includes etching predetermined patterns into various layers of material formed during fabrication of the device. This process is referred to herein as "patterning and etching." Photolithography and reactive ion etching, for example, are commonly used pattern and etch processes. These or other pattern and etch processes, well known to those skilled in the art, may be used to implement the present invention.

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Reference will now be made to Figs. 4-7, which illustrate the general structure of one embodiment of the invention without regard to the specific type of semiconductor device into which the invention might be incorporated. Figs. 11-16, which are discussed later, illustrate one preferred application for the invention wherein the invention is incorporated into a stacked capacitor DRAM.

Referring to Fig. 4, insulating layer 23 and underlayer 20 have been formed over substrate 22. Underlayer 20 is patterned and etched to form opening 24. Opening 24 need not be etched all the way through underlayer 20. All that is required is a step opening in underlayer 20. A layer of conductive material 26 is then formed over underlayer 20 and in opening 24 as shown in Fig. 5. Insulating layer 23 is provided to prevent electrical shorting between conductive layer 26 and substrate 22. If shorting between conductive layer 26 and substrate 22 is not a problem, then insulating layer 23 may be omitted. Other layers may also be formed between substrate 22 and underlayer 20. Overlayer 28 is then formed on conductive layer 26.

Referring to Fig. 6, overlayer 28 is patterned and etched to form contact hole 30. Conductor 32 is then formed in contact hole 30 as shown in Fig. 7. Typically, underlayer 20 will be made of an insulating material such as silicon dioxide or a composite stack of conducting and insulating materials. Conductive layer 26 is doped polysilicon and overlayer 28 is boro-phospho-silicate glass (BPSG) or other suitable insulating material. Although the relative thicknesses of conductive layer 26 and overlayer 28 are not critical to the invention, the objectives of the invention are better realized where, as in most semiconductor applications, overlayer 28 is much thicker than conductive layer 26.

Opening 24 is sized and shaped to form localized thick region 34 in conductive layer 26 within opening 24. Opening 24 and thick region 34 are formed subjacent to contact hole

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30, that is, below and adjacent to contact hole 30. Opening 24 and thick region 34 are preferably positioned directly below contact hole 30 as shown in Fig. 6, although a reliable contact will be made even in the event of substantial misalignment of contact hole 30 to opening 24. In this embodiment, the width (or diameter) of opening 24 is less than or equal to twice the product of the thickness of conductive layer 26 at surface 38 of underlayer 20 adjacent to opening 24 and the Conformality of the conductive material. Thus, for conductive material having Conformality C and thickness T, the width W of opening 24 is determined from the following equation:  $W \leq 2 \times T \times C$ . In this way, conductive layer 26 will completely fill opening 24. Unless otherwise noted, the "thickness" of a layer of material, as used herein, refers to the thickness measured in a direction parallel to the longitudinal axis describing the depth of the contact hole. Hence, for the orientation of the layers of material illustrated in the drawings, "thickness" refers to the vertical thickness of the material.

The Conformality of a particular material, as is well known in the art, represents the comparative rate at which a material is simultaneously deposited along the top surface and sidewall of an opening or "step" in the underlying material. Conformality is defined by the ratio of the thickness of the deposited material along the sidewall of a step in the underlying material and its thickness along the surface adjacent to the step. Polysilicon, for example, has a Conformality of about 0.80. If conductive layer 26 is made of polysilicon having a thickness of 1,500 angstrom at surface 38 of underlayer 20, then the width of opening 24 preferably is less than or equal to 2,400 Angstroms ( $2 \times 1,500$  Angstroms  $\times 0.80$ ). This will ensure conductive layer 26 completely fills opening 24 to form a robust thick region 34. Thick region 34 allows for a reliable contact to conductor 32 even

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in the event of a substantial contact hole overetch as shown in Fig. 7.

Opening 24 should be deep enough so that thick region 34 is sufficiently thick to accommodate anticipated overetching of contact hole 30. Overetching, as applied herein to contact hole 30, refers to the continuation of the etch after contact hole 30 has reached the nominal depth of conductive layer 26 below overlayer 28. In many semiconductor device applications, overlayer 28 will be formed over a structure having a stepped topography, resulting in variations in the thickness of overlayer 28. The thickness of overlayer 28 may also vary due to non-uniformity in deposition and planarization processes. Contact hole 30 must overetched as necessary to account for such variations. Other factors may also effect the contact hole etch. For example, the contact hole may be etched simultaneously with a deeper bit line contact as in the stacked capacitor DRAM described below. In this example, the etch must continue until the deeper bit line contact is reached, resulting in a substantial overetch of contact hole 30.

In general, the depth of opening 24 will depend upon the nominal depth of contact hole 30, the total effective depth of the etch during which contact hole 30 is formed, and the selectivity of the etch. The total effective depth of this etch will be determined by the depth of the deepest contact being etched and any overetch of that deep contact. Selectivity is a measure of the etch rate of the target material (overlayer 28 in this example) relative to other materials of interest exposed to the etchant (conductive layer 26). Selectivity is defined by the following equation:  $S_{AB} = E_A/E_B$ , where  $E_A$  is the etch rate of the target material to be etched and  $E_B$  is the etch rate of the second material of interest exposed to the etchant. For a contact hole having a nominal depth  $D_{CH}$ , a total etch depth  $D_{TE}$ , and etch selectivity  $S$ , the thickness  $T_{TR}$  of thick region 34 is determined according

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to the following equation:  $T_{IR} \geq (D_{TE}-D_{CH})/S$ . The corresponding depth  $D_o$  of opening 24 is determined according to the following equation:  $D_o \geq (D_{TE}-D_{CH})/S - T_{CL}$ , where  $T_{CL}$  is the thickness of conductive layer 26.

5 In another embodiment of the invention, illustrated in Figs. 8-10, the localized thick region is formed as a spacer on the sidewall of the opening. Referring to Fig. 8, insulating layer 23 and underlayer 20 having opening 24 therein have been formed on substrate 22. Conductive layer  
10 26 is formed over underlayer 20 and along the surfaces of opening 24, to form localized thick regions 34 along the sidewalls 36 of opening 24. Overlayer 28 is then formed on conductive layer 26.

15 Referring to Figs. 9 and 10, overlayer 28 is patterned and etched to form contact hole 30. Fig. 9 is a cross section view taken along the line 1-1 in Fig. 10. In the top down plan view of Fig. 10, however, overlayer 28 has been removed to better illustrate the features of this embodiment of the invention. Contact hole 30 is thereafter filled with a conductor (not shown) to contact conductive layer 26 at thick region 34. In this embodiment, the width of opening 24 is not critical nor is it necessary that contact hole 30 be precisely aligned to opening 24. In practice, the structure illustrated  
20 in Figs. 8-10 may be formed by design or this structure may result from overetching and/or misalignment of contact hole 30 in the structure shown in Fig. 6. The invention thus provides a reliable contact while allowing for generous etching and alignment tolerances.

25 Reference will now be made to Figs. 11-16, which illustrate application of the present invention to a stacked capacitor DRAM. Referring first to Fig. 16, one memory cell in a memory cell array region 94 of wafer 50 is shown on the left side of Fig. 16, including capacitor 96 and field effect access transistor 98. Metal conductor 95 contacting cell poly  
30 80 at contact area 99 in a peripheral region 97, typically

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located immediately adjacent to the array region, is shown on the right side of Fig. 16. The components of the device illustrated in Fig. 16 and the process for making those components will be described with reference to Figs. 11-15.

Referring to Fig. 11, wafer 50 comprises a lightly doped p-type single crystal silicon substrate 52 which has been oxidized to form thin gate insulating layer 54 and thick field oxide region 56. This application of the invention will be described using lightly doped p-type silicon as the starting material, although the invention may be implemented with other substrate materials. If other substrate materials are used, then there may be corresponding differences in materials and structure of the device as is well known in the art. Field oxide region 56 is formed by conventional methods well known in the art, such as forming an apertured layer of silicon nitride (not shown) or other non-oxidizable material on the surface of substrate 52 and thereafter oxidizing the exposed portions of the substrate. Thin gate insulating layer 54 is formed by thermally growing or depositing silicon dioxide on the surface of substrate 52. First polysilicon layer 58, tungsten silicide layer 60 and silicon dioxide layer 62 are then deposited or "stacked" over substrate 52. First polysilicon layer 58, tungsten silicide layer 60 and silicon dioxide layer 62 are referred to jointly as underlayer 64.

Referring to Fig. 12, underlayer 64 is patterned and etched to form transistor gate electrode 66 in the array and opening 68 in the periphery. These layers are deposited, patterned and etched using conventional methods well known in the art. Alternatively, gate electrode 66 and opening 68 may be formed in a single layer of polysilicon deposited and etched as describe above or other combinations of conductors and insulators may be used. The tungsten silicide and silicon dioxide layers are included herein simply to better illustrate the details of one of the preferred embodiments of the invention. Source/drain regions 70a and 70b are formed in the

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array by implanting n-type impurities, typically phosphorous or arsenic atoms, into substrate 52 on opposite sides of gate electrode 66.

Referring to Fig. 13, insulating layer 71, typically made of silicon dioxide, is stacked over substrate 52. Referring to Fig. 14, insulating layer 71 is patterned and etched to form spacers 72. A second polysilicon layer 73 is then stacked over substrate 52 and patterned and etched to form capacitor bottom electrode 74. Capacitor dielectric layer 76, typically made of silicon nitride, is stacked over substrate 52. A third polysilicon layer is then stacked over substrate 52 and patterned and etched to form capacitor top electrode 80, also commonly referred to as the "cell poly", as shown in Fig. 15, and this etch may continue down through dielectric layer 76. Thus, a first region 82 of cell poly 80 is formed in the array over bottom electrode 74 and a second region 84 of cell poly 80 has been formed in the periphery for subsequent connection to a metal conductor.

Referring again to Fig. 14, opening 68 (shown in Figs. 12 and 13) has now been filled with spacers 72, second polysilicon layer 73, dielectric layer 76 and cell poly 80. Opening 68 is sized and shaped to form localized thick region 86 in cell poly 80 within opening 68. To ensure that cell poly 80 bridges the gap in opening 68 to form localized thick region 86, the width of opening 68 should be no greater than the combined widths of spacers 72, second polysilicon layer 73, dielectric layer 76 and cell poly 80 within opening 68. The width of each of these materials within opening 68 is proportional to the thickness at which those materials are formed along the surface of underlayer 64 adjacent to opening 68. The width of opening 68 can, therefore, be determined according to the following equation, where insulating layer 71 has a thickness  $T_I$  and Conformality  $C_I$ , second polysilicon layer 73 has thickness  $T_{PL}$  and Conformality  $C_{PL}$ , dielectric layer 76 has a thickness  $T_d$  and Conformality  $C_d$ , and cell poly

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80 has a thickness  $T_{CP}$  and Conformality  $C_{CP}$ :  $W \leq 2 \times ((T_I \times C_I) + (T_{PL} \times C_{PL}) + (T_D \times C_D) + (T_{CP} \times C_{CP}))$ . Of course, if the width of each layer of material lying within opening 68 is otherwise known or can be determined directly, then the above described equation need not be applied. In general, however, the width an opening having multiple layers of materials deposited therein can be determined according to the following equation:  
5  $W \leq \sum_{i=1}^N 2 \times T_i \times C_i$ , where each layer has a thickness  $T_i$  as measured along the surface adjacent to the opening, and  
10 Conformality  $C_i$ .

Assuming a 4 Mbit DRAM having an access transistor gate about  $0.6 \mu\text{m}$  wide, silicon dioxide insulating layer 71 has a thickness  $T_I$  of approximately 3,000 Angstroms and Conformality  $C_I$  of 0.67, second polysilicon layer 73 has a thickness  $T_{PL}$  of approximately 2,000 Angstroms and Conformality  $C_{PL}$  of 0.80, dielectric layer 76 has a thickness  $T_D$  of approximately 100 Angstroms and Conformality  $C_D$  of 0.90, and cell poly 80 has a thickness  $T_{CP}$  of approximately 1,000 Angstroms and Conformality  $C_{CP}$  of 0.80. Therefore, opening 68 preferably is no more than 20 9,000 Angstroms wide.

Referring to Fig. 15, overlayer layer 88, made of boro-phospho-silicate glass (BPSG) or other suitable insulator, is stacked over substrate 52. Overlayer 88 is patterned and etched to form bit line contact 90 in the array and contact hole 92 in the periphery. Opening 68 (shown on Fig. 12) is positioned directly below contact hole 92. Ideally, the contact hole etch will end on the surface of cell poly 80. As a practical matter, and due to the variations in the thickness of overlayer 88 and the greater depth of the bit line contact 90, contact hole 92 is typically over etched to ensure bit line contact 90 is etched to substrate 52. Consequently, the contact hole etch usually extends into the surface of cell poly 80, as illustrated in Fig. 15. The device structure is completed as shown in Fig. 16 using metallization processes well known in the art.

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There has been shown and described a novel semiconductor device wherein a conductive layer has a localized thick region formed and positioned below the contact hole, thus eliminating the risk of etching the contact hole through the thin conductive layer. The particular embodiments shown in the drawings and described herein are for purposes of example and should not be construed to limit the invention as set forth in the appended claims. Those skilled in the art may now make numerous uses and modifications of the specific embodiments described without departing from the scope of the invention. For instance, the invention could be readily incorporated into trench capacitor DRAMs, Static Random Access Memories (SRAMs), logic circuit semiconductor devices and other such devices where a contact via is formed on a layer of relatively thin conductive material. The process steps described may in some instances be performed in a different order and/or equivalent structures and processes may be substituted for the various structures and processes described.

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I claim:

1. A semiconductor device having an improved contact to a conductive layer, comprising:

a. a first layer of conductive material;

5 b. a second layer of material having a contact hole therethrough on the first layer;

c. a localized thick region in the first layer subjacent the contact hole; and

10 d. a conductor contacting the thick region through the contact hole.

2. A semiconductor device according to Claim 1, wherein the thick region is positioned directly below the contact hole.

3. A semiconductor device having an improved contact to a conductive layer, comprising:

15 a. an underlayer of material having an opening therein;

b. a layer of conductive material formed on the underlayer and in the opening;

20 c. an overlayer of material on the layer of conductive material, the overlayer having a contact hole etched therethrough;

d. the opening being positioned, sized and shaped to form a localized thick region in the layer of conductive material subjacent the contact hole; and

25 e. a conductor contacting the thick region through the contact hole.

4. A semiconductor device according to Claim 3, wherein:

- the conductive material has a Conformality C;
- the layer of conductive material has a thickness  $T_1$  at a location along a surface of the underlayer adjacent the opening;
- the opening has a width W, where the width of the opening is determined from the equation:  $W \leq 2 \times T_1 \times C$ .

5. A semiconductor device according to Claim 4, wherein the conductive material is polysilicon having a conformality C of about 0.80.

10 6. A semiconductor device according to Claim 3, wherein the etch of the overlayer has a selectivity S with respect to the conductive layer and extends to a total effective depth  $D_{TE}$ , the contact hole has a nominal depth  $D_{CH}$ , the layer of conductive material has a thickness  $T_{CL}$  and the opening has a depth D, where D is determined from the equation:  $D \geq (D_{TE} - D_{CH}) / S - T_{CL}$ .

15 7. A semiconductor device according to Claim 6, wherein the selectivity S is determined from the equation:  $S = E_o / E_c$ , where  $E_o$  is the rate at which the overlayer is etched and  $E_c$  is the rate at which the conductive layer is etched.

20 8. A semiconductor device according to Claim 3, wherein the etch of the overlayer has a selectivity S and extends to a total effective depth  $D_{TE}$ , the contact hole has a nominal depth  $D_{CH}$  and the thick region has a thickness  $T_{TR}$ , where  $T_{TR}$  is determined from the equation:  $T_{TR} \geq (D_{TE} - D_{CH}) / S$ .

9. A semiconductor device according to Claim 8, wherein the selectivity S is determined from the following equation:  $S = E_o/E_c$ , where  $E_o$  is the rate at which the overlayer is etched and  $E_c$  is the rate at which the conductive layer is etched.

5       10. A semiconductor device according to Claim 3, further comprising a capacitor having a bottom electrode and a top electrode electrically isolated from the bottom electrode by a dielectric layer, wherein the layer of conductive material forms the top electrode and the conductor forms a contact through which a reference voltage is applied to the top electrode.

10       11. A semiconductor device, comprising:

15       a. a field effect transistor formed in a memory cell array region of a semiconductor substrate, the field effect transistor comprising a gate electrode formed on the substrate, and first and second source/drain regions formed in the surface of the substrate on opposite sides of the gate electrode;

20       b. a capacitor formed in the memory cell array region, the capacitor comprising a bottom electrode formed on the substrate in electrical contact with the first source/drain region, a dielectric layer formed on the bottom electrode, and a first region of a polysilicon top electrode formed on the dielectric layer over the bottom electrode; —

25       c. a second region of the polysilicon top electrode formed in a peripheral region of the substrate adjacent to the memory cell array region;

30       d. an underlayer of material interposed between the substrate and the second region of the polysilicon top electrode in the peripheral region, the underlayer having an opening therein;

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e. an insulating layer formed on the second region of the polysilicon top electrode, the insulating layer having a contact hole therethrough;

5 f. a conductor contacting the second region of the polysilicon top electrode through the contact hole; and

g. wherein the opening is positioned below the contact hole.

10 12. A semiconductor device according to Claim 11, further comprising a localized thick region in the second region of the polysilicon top electrode within the opening subjacent the contact hole.

15 13. A process for making a semiconductor device having an improved contact to a conductive layer, comprising the steps of:

a. forming a first layer of conductive material;

b. forming a second layer of material having a contact hole therethrough on the first layer;

c. forming a localized thick region in the first layer subjacent the contact hole; and

20 d. forming a conductor contacting the thick region through the contact hole.

14. A process for making a semiconductor device having an improved contact to a conductive layer, comprising the steps of:

25 a. forming an underlayer of material having an opening therein;

b. forming a layer of conductive material on the underlayer and in the opening;

30 c. forming an overlayer of material on the layer of conductive material and etching a contact hole therethrough;

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d. forming a localized thick region in the layer of conductive material within the opening subjacent the contact hole; and

5 e. forming a conductor contacting the thick region through the contact hole.

15. A process for making a semiconductor device according to Claim 14, wherein:

a. the conductive material has a Conformality C;

10 b. the layer of conductive material has a thickness  $T_1$  at a location along a surface of the underlayer adjacent the opening;

c. the opening has a width W; and

15 d. the width of the opening is determined from the equation:  $W \leq 2 \times T_1 \times C$ .

16. A process for making a semiconductor device according to Claim 14, wherein the etch of the overlayer has a selectivity S with respect to the conductive layer and extends to a total effective depth  $D_{TE}$ , the contact hole has a nominal depth  $D_{CH}$ , the layer of conductive material has a thickness  $T_{CL}$  and the opening has a depth D, where D is determined from the equation:  $D \geq (D_{TE} - D_{CH})/S - T_{CL}$ .

20  
25 17. A process for making a semiconductor device according to Claim 16, wherein the selectivity S is determined from the following equation:  $S = E_o/E_c$ , where  $E_o$  is the rate-at which the overlayer is etched and  $E_c$  is the rate at which the conductive layer is etched.

18. A process for making a semiconductor device according to Claim 14, wherein the etch of the overlayer has a selectivity S and extends to a total effective depth  $D_{TE}$ , the contact hole has a nominal depth  $D_{CH}$  and the thick region has a thickness  $T_{TR}$ , where  $T_{TR}$  is determined from the equation:  $T_{TR} \geq (D_{TE} - D_{CH}) / S$ .

5           19. A process for making a semiconductor device according to Claim 18, wherein the selectivity S is determined from the following equation:  $S = E_o/E_c$ , where  $E_o$  is the rate at which the overlayer is etched and  $E_c$  is the rate at which the conductive layer is etched.

10

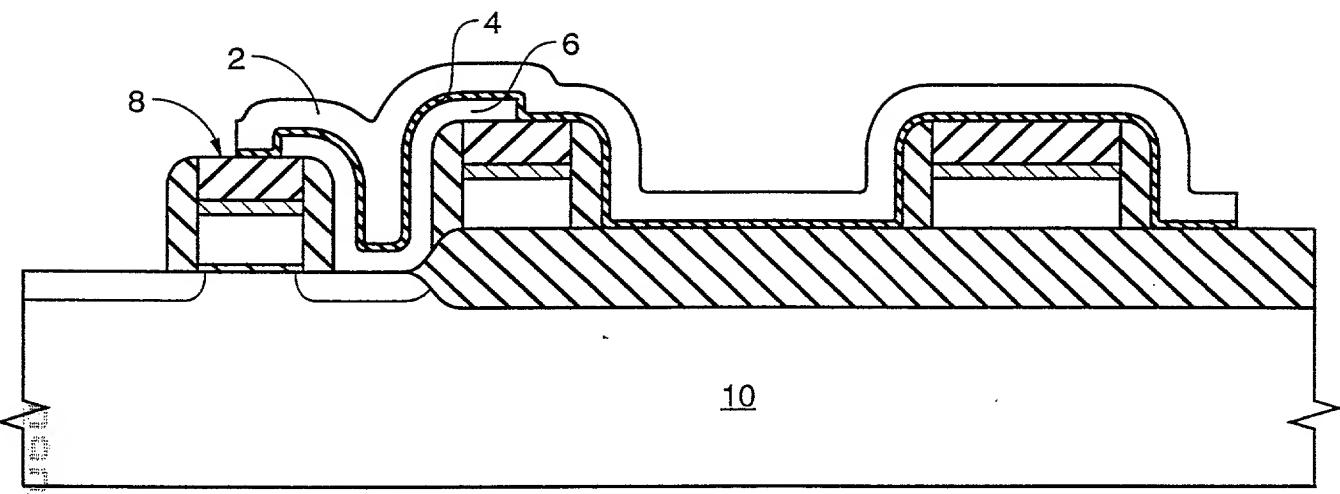
15

20. A process for making a semiconductor device according to Claim 14, further comprising the steps of forming a capacitor having a bottom electrode and a top electrode electrically isolated from the bottom electrode by a dielectric layer, wherein the layer of conductive material forms the top electrode and the conductor forms a contact through which a reference voltage is applied to the top electrode.

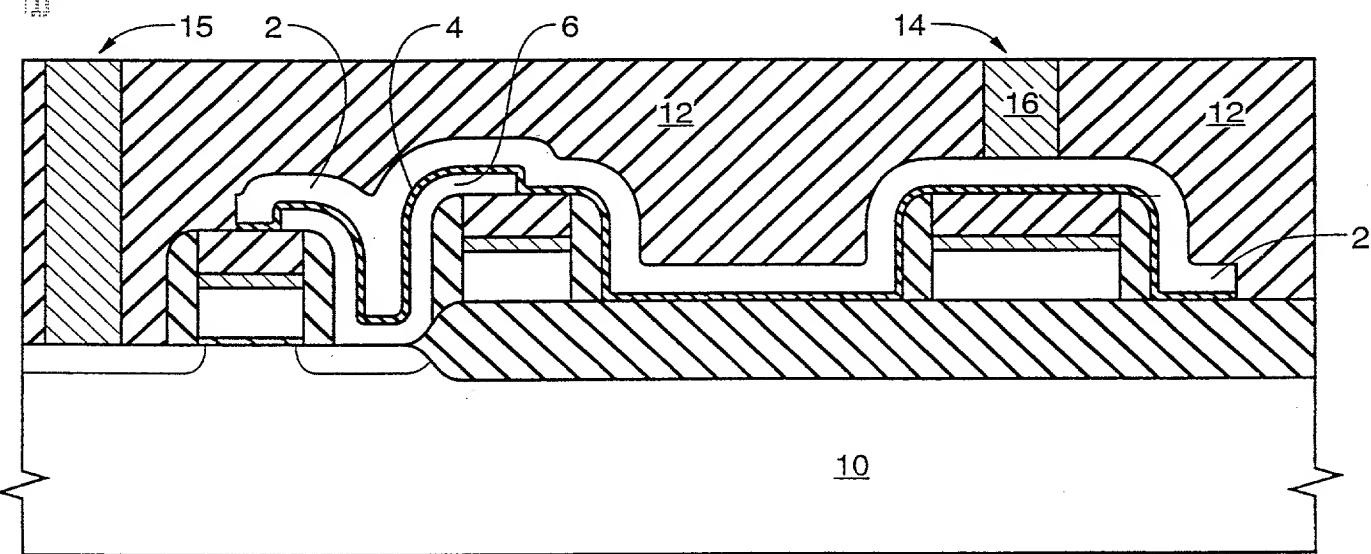
Inventor(s) : H. Rhodes

**ABSTRACT**

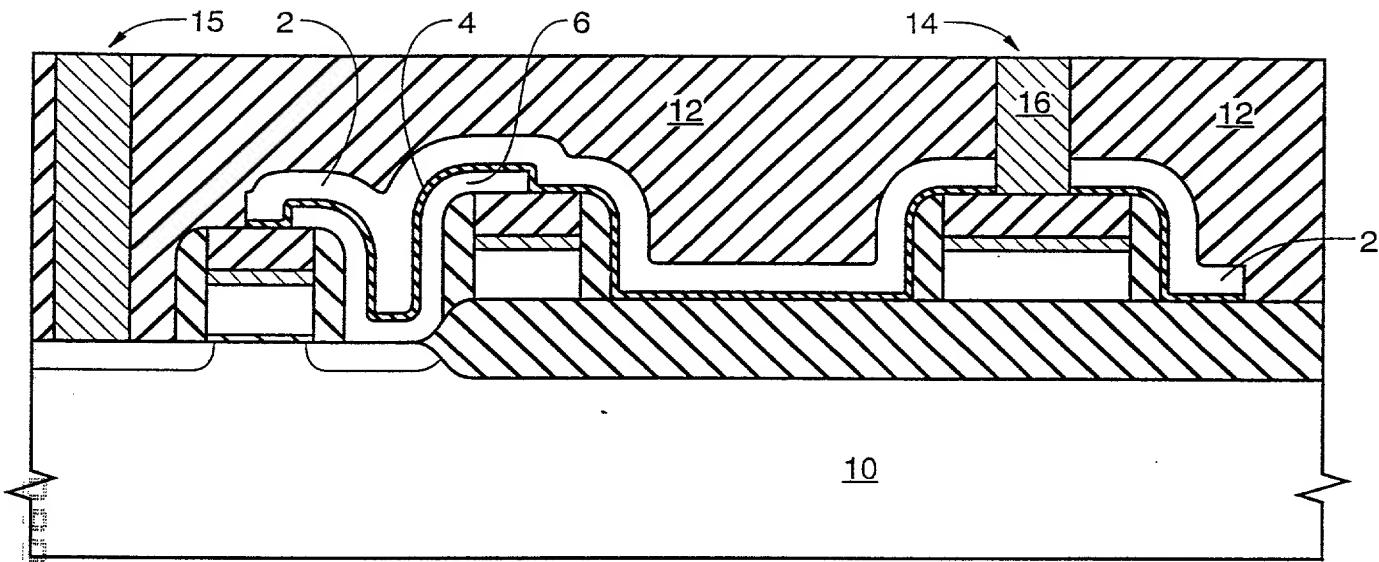
A semiconductor device and fabrication process wherein the device includes a conductive layer with a localized thick region positioned below the contact hole. In one embodiment of the invention, the thick region to which contact is made is formed by means of an opening in an underlayer of material. This embodiment of the device includes an underlayer of material having an opening therein; a layer of thin conductive material formed on the underlayer and in the opening; an overlayer of material having a contact hole therethrough formed on the layer of thin conductive material; a conductor contacting the layer of thin conductive material through the contact hole; and wherein the opening in the underlayer is positioned below the contact hole and sized and shaped to form a localized thick region in the layer of thin conductive material within the opening.



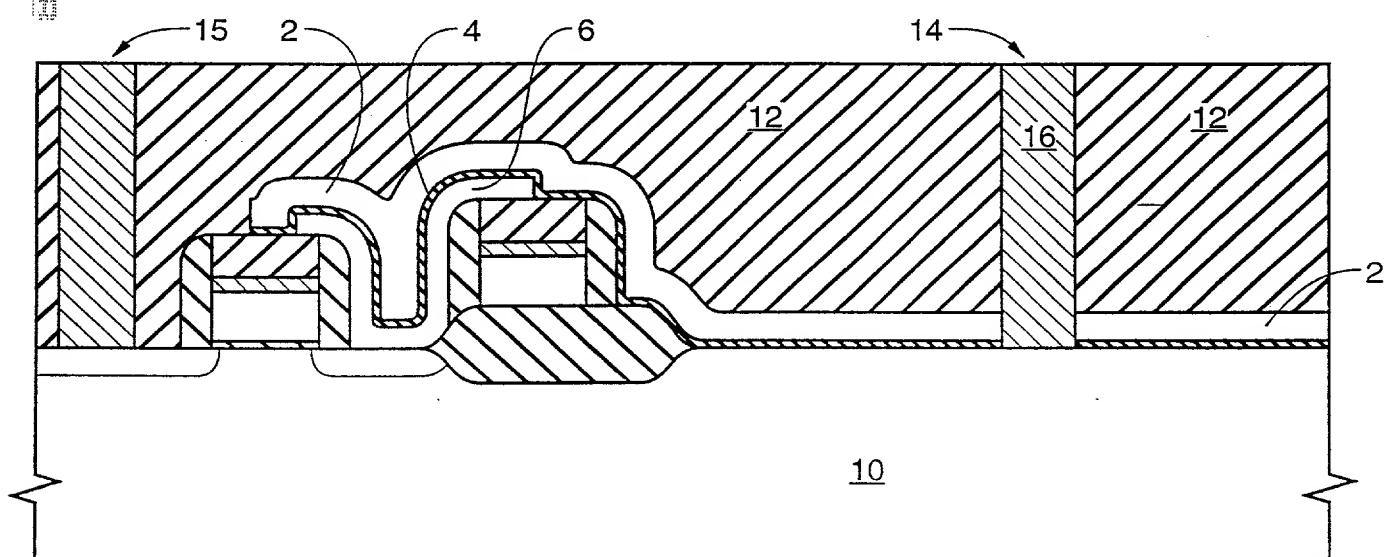
**FIG. 1**  
(PRIOR ART)



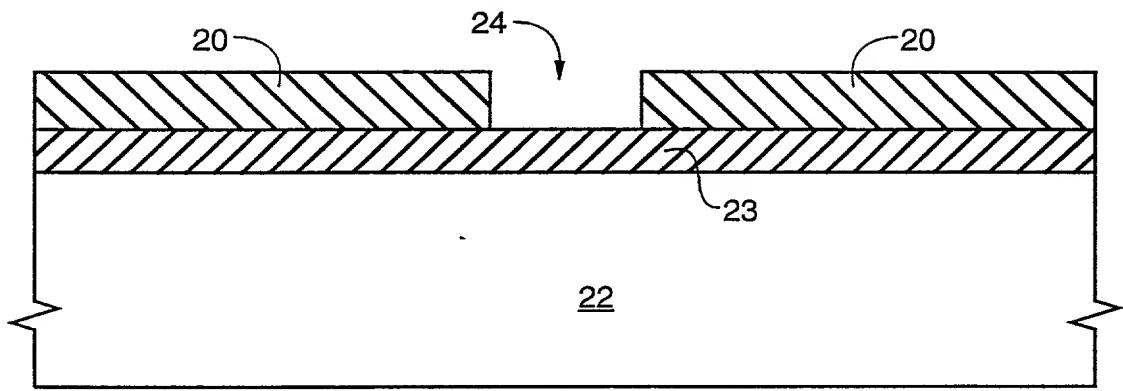
**FIG. 2**  
(PRIOR ART)



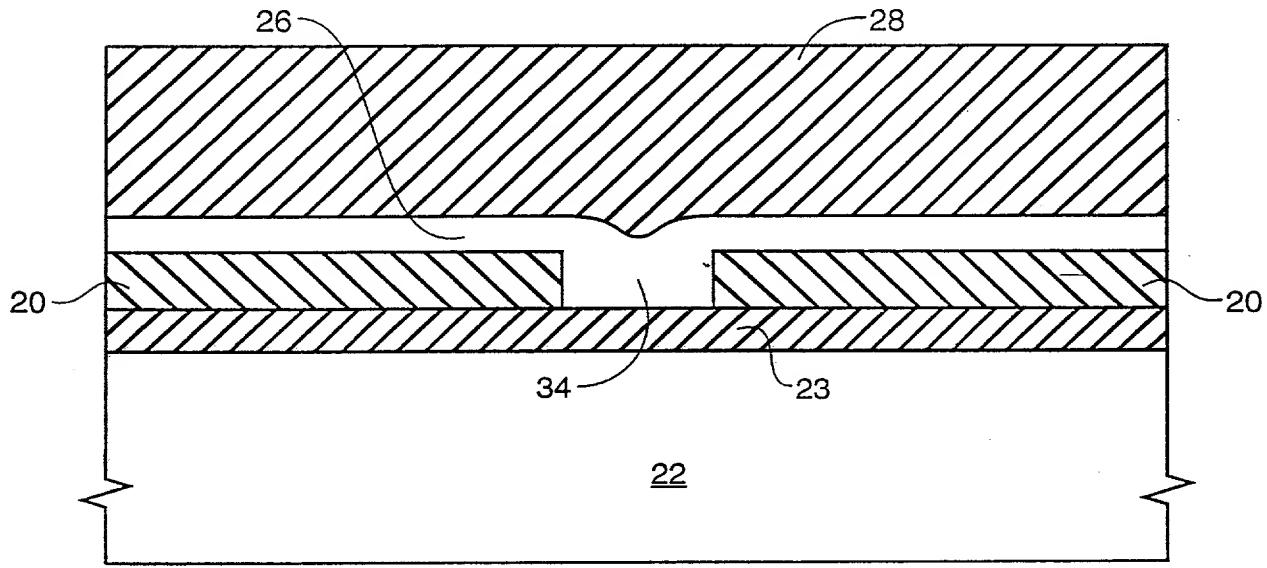
**FIG. 3A**  
(PRIOR ART)



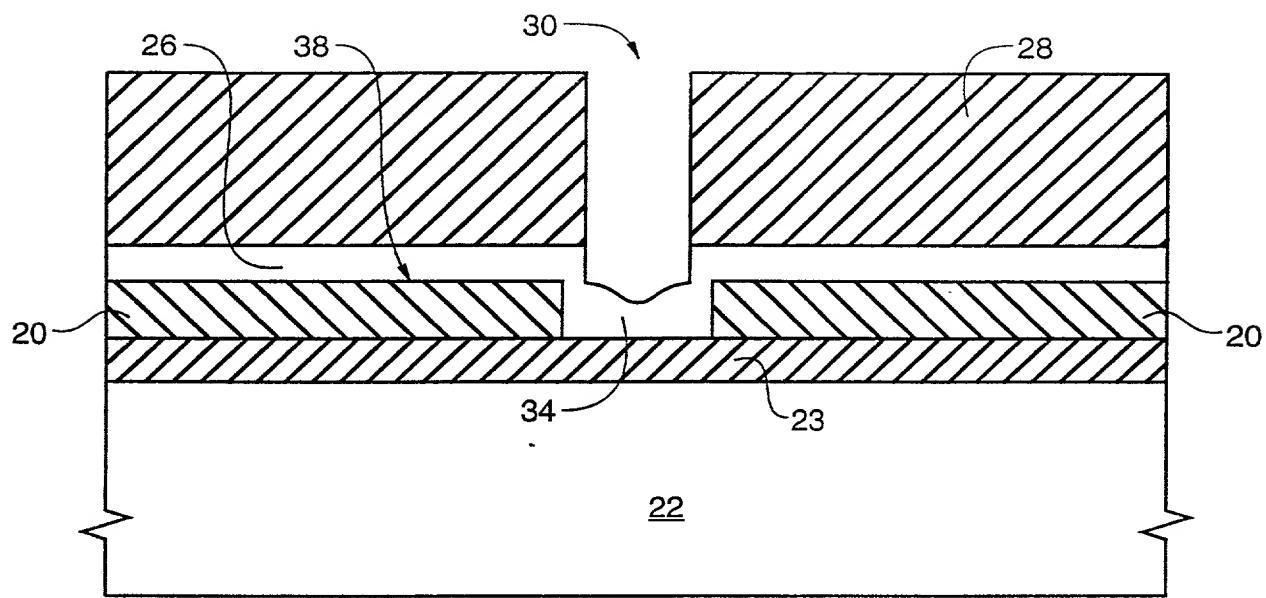
**FIG. 3B**  
(PRIOR ART)



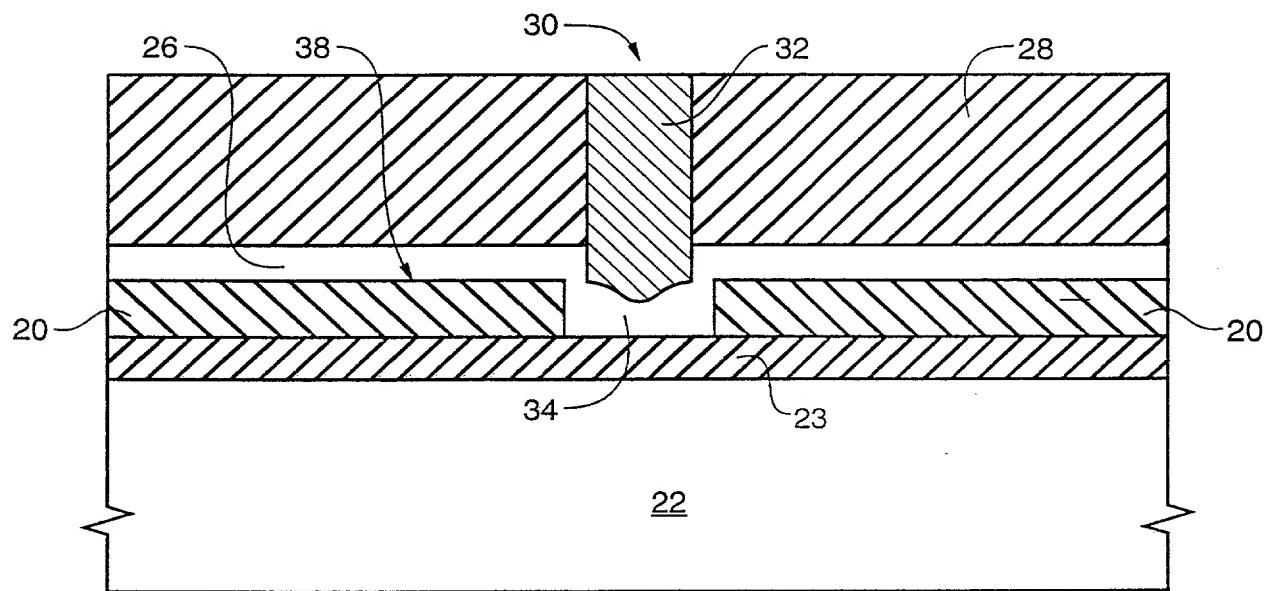
**FIG. 4**



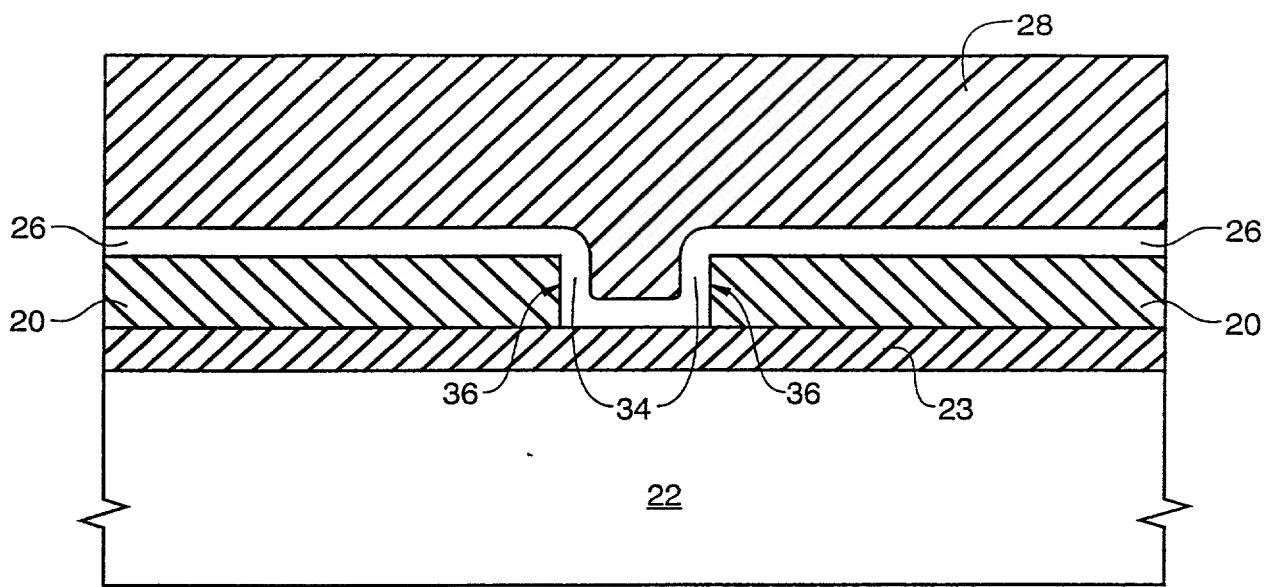
**FIG. 5**



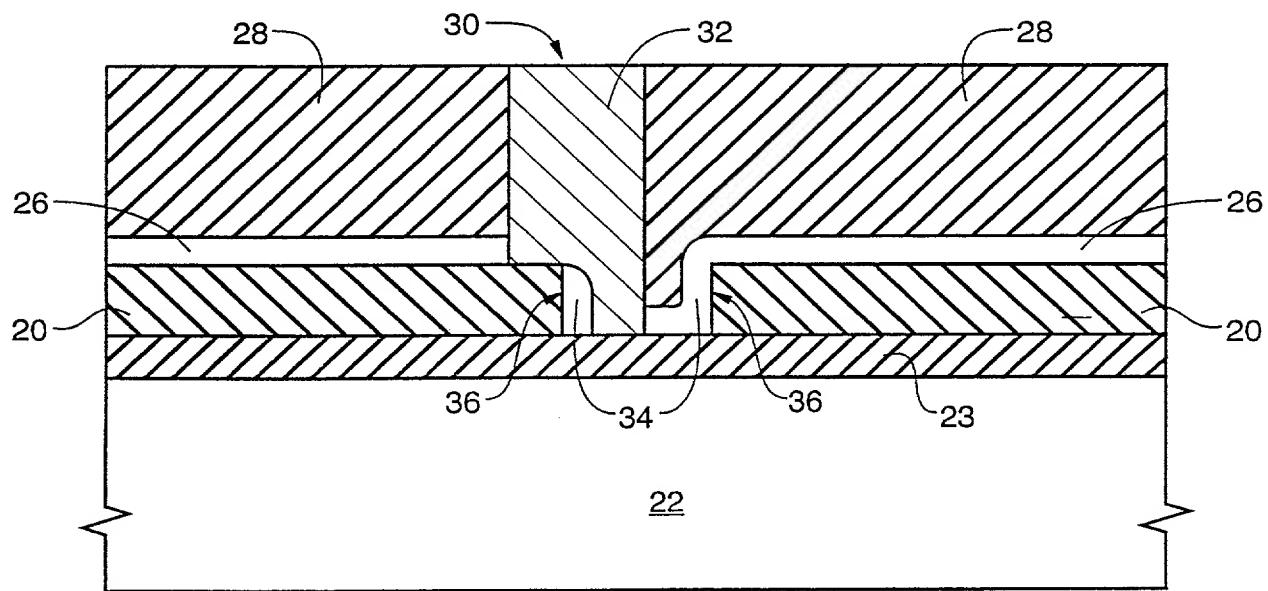
**FIG. 6**



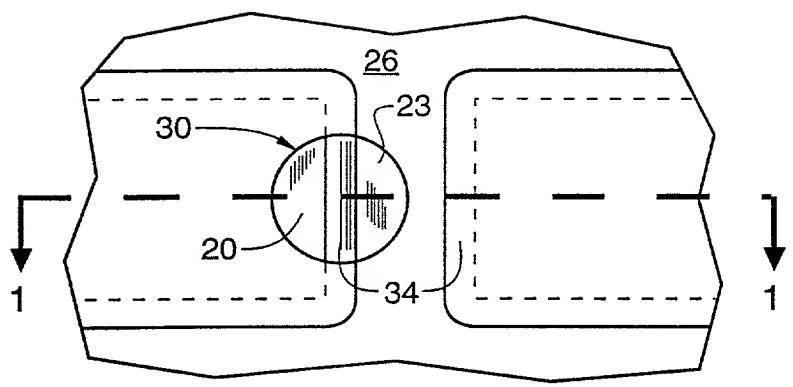
**FIG. 7**



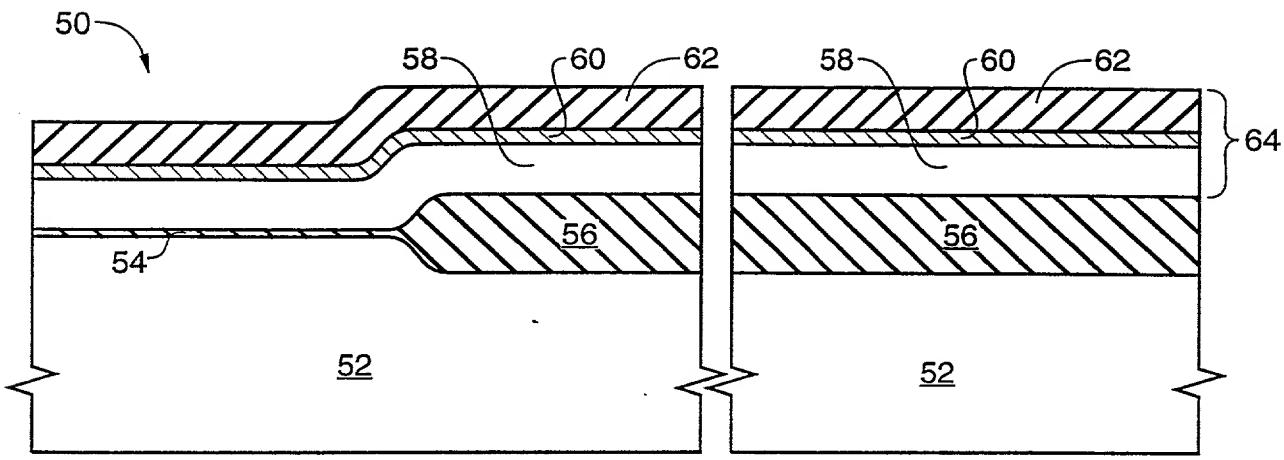
**FIG. 8**



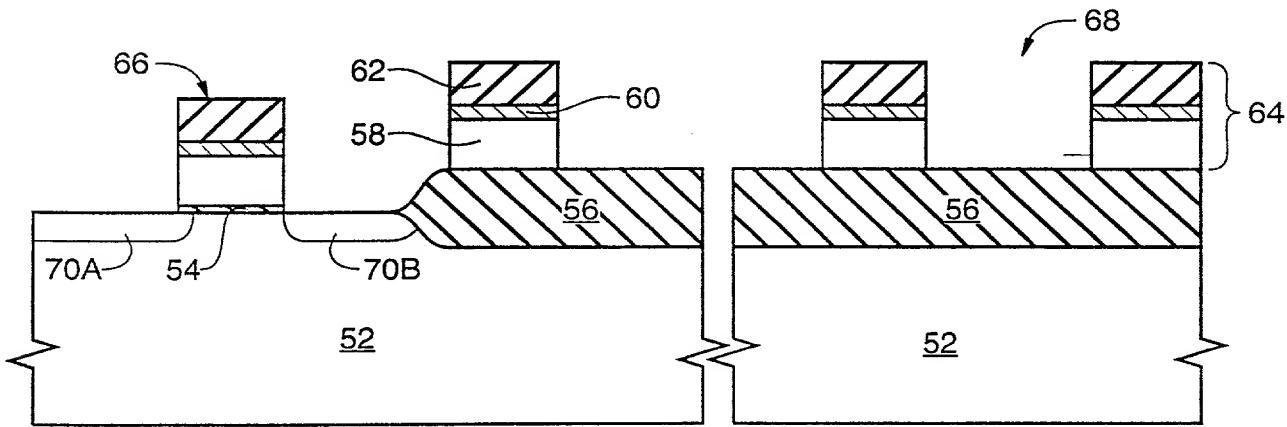
**FIG. 9**



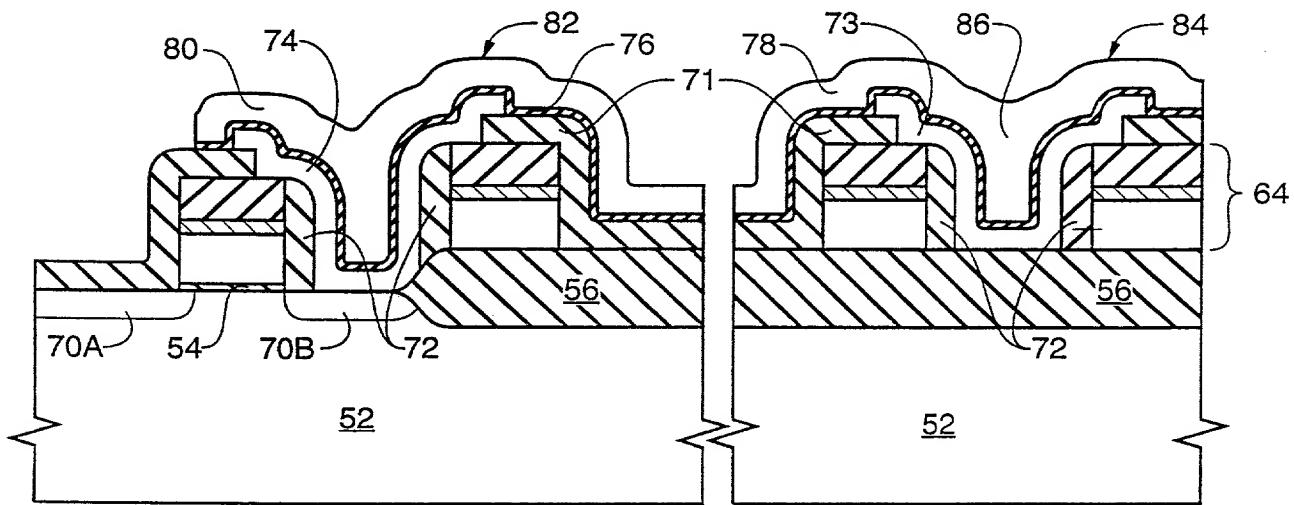
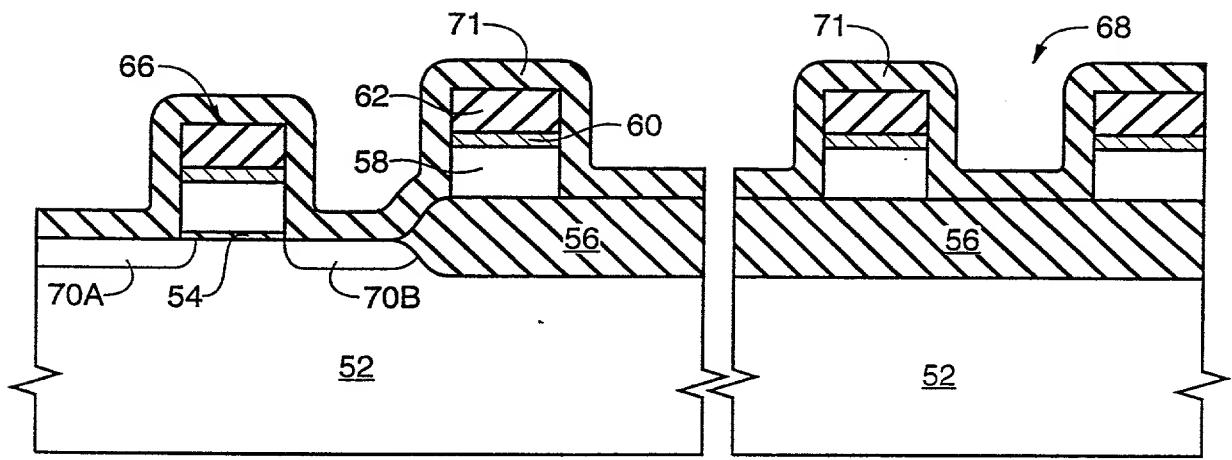
**FIG. 10**

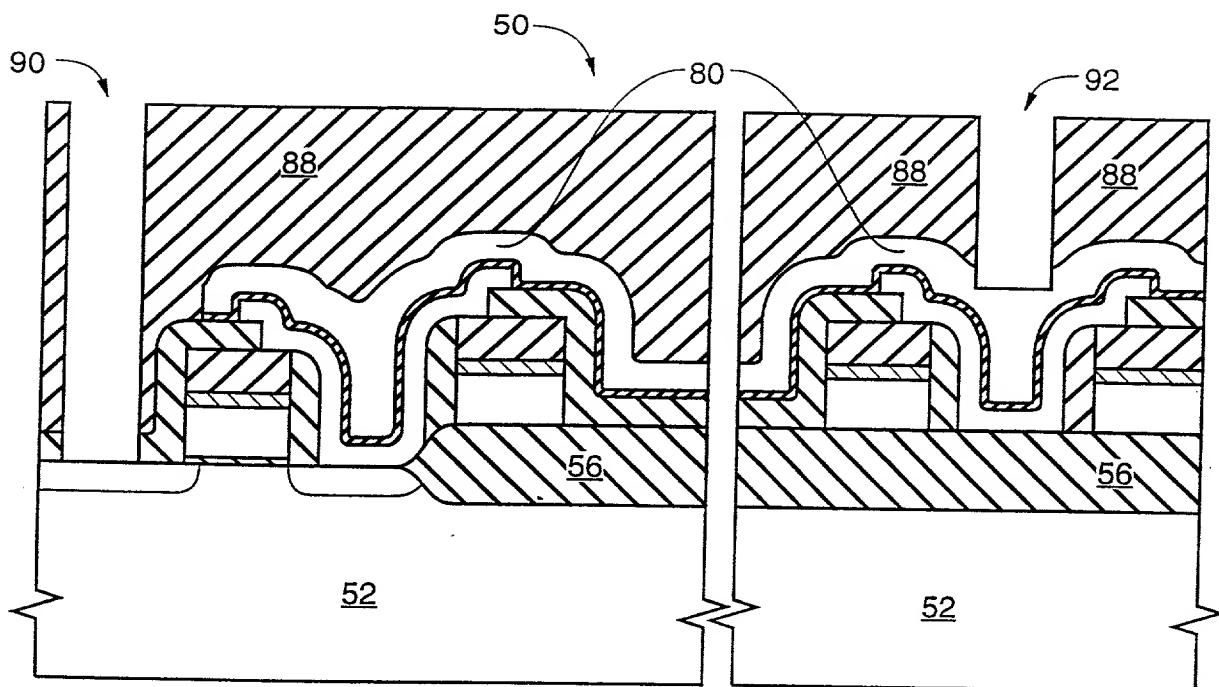


**FIG. 11**

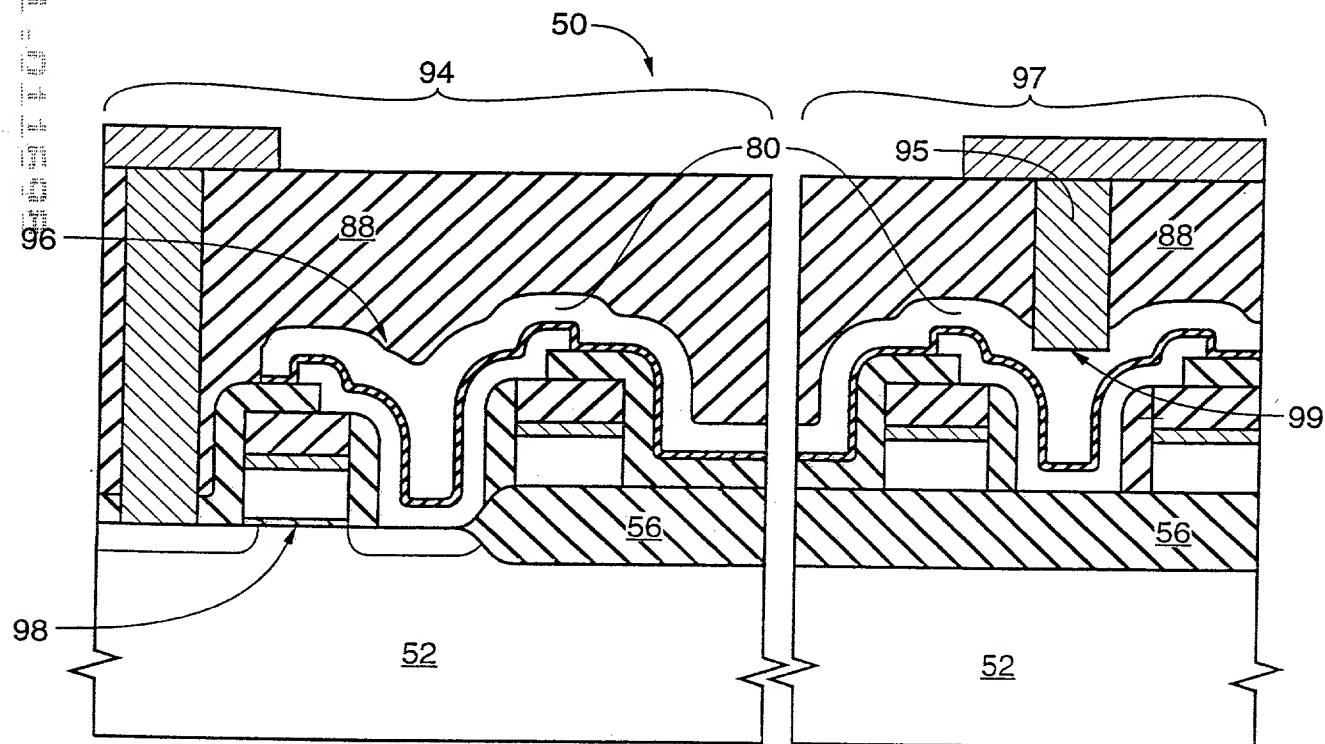


**FIG. 12**





**FIG. 15**



**FIG. 16**

**DECLARATION AND POWER OF ATTORNEY**

As below named inventor, I hereby declare that:

My residence, post office address and citizenship is as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled; **SEMICONDUCTOR DEVICE HAVING IMPROVED CONTACTS TO A THIN CONDUCTIVE LAYER AND PROCESS FOR MAKING SAID DEVICE**; the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: **NONE**.

I hereby claim the benefit under Title 35, United States Code Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application: **NONE**.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As the named inventor, I appoint the following as attorneys or agents to transact all business in the Patent and Trademark Office for this application -- Steven R. Ormiston (Registration No. 35,974), Angus C. Fox (Registration No. 31,828), and David J. Paul (Registration No. 34,692).

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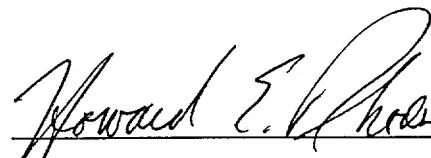
Inventor's Full Name:

Inventor's Signature:

Citizenship:

Post Office Address:

City, State and  
Country of Residence:

 Date: 2-28-95

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Boise, Idaho, 83706 United States of  
America